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FOR

LOW DISTORTION CURRENT SWITCHES FOR HIGH SPEED CURRENT STEERING DIGITAL-TO-ANALOG CONVERTERS

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to current steering digital to analog converters (DACs).

2. Prior Art

A thermometer-coded DAC consists of a large number of equal value current sources. These are each switched between the two DAC outputs using differential pairs, as shown in Figure 1. The differential pair transistors M_1 and M_2 are operated in saturation, and each have a voltage gain equal to $G_{SW} = g_m/g_{ds}$ when on. At any one time, one of these transistors is on, and the other is off.

There is a parasitic capacitance C_S associated with the common source node of each differential pair. The potential on the common source node of the differential pair can be called V_{CS}. The output of the DAC has a common mode voltage V_{CM} and a differential voltage V_O. When the voltage at the output of the transistor that is on changes by ΔV_O, the settled voltage at the common source node V_{CS} is changed by a

factor $\Delta V_O \cdot g_{ds}/g_m$. The current required to charge and discharge the capacitance C_S is taken from the current source (signal current). It can be shown that this results in third order harmonic distortion for a differential output, as well as second order harmonic distortion for a single ended output. The amount of distortion is a function of output frequency, and the number of segmented bits, among other things.

The previously known methods available to minimize the distortion caused by the parasitic capacitance C_S of the differential pair common source node may be summarized as follows:

1. The capacitance C_S itself can be minimized. This is done by using switches that are as small as possible. The current source is typically implemented as a PMOS cascode current source. By locating the cascode transistor of the current source close to the switch common source node, the parasitic capacitance associated with routing between current source and switch can be minimized. Minimizing the width of the switch transistors M_1 and M_2 results in a high current density in these transistors, resulting in large gate voltage overdrive. This reduces the voltage drop available for the current sources, reducing the allowable gate voltage overdrive on the current sources. Thus, the sensitivity of

the DAC currents to device mismatch is increased, resulting in degraded static linearity. Another way to optimize this is to build the DAC core from NMOS devices instead of PMOS devices. These typically have an advantage due to the higher electron mobility, allowing the designer to make the devices smaller by roughly a factor of 3.

2. The voltage gain of the switch transistors can be optimized. This voltage gain is limited by the g_m/g_{ds} of the switches. If the voltage gain is increased by increasing the channel length, the C_{GS} also increases - hence not much can be gained in terms of distortion using only this method. Selecting a process with high g_m/g_{ds} - e.g. a BiCMOS process - using bipolar transistors as data switches, is one way to achieve this.

3. Regulating the cascode of the current source. This enhances the output impedance of the current source. Since the majority of the capacitance C_S is associated with the switch transistors, this does not help third harmonic distortion much, but may be advantageous for static linearity and intermodulation distortion.

4. Bootstrapping the bulk of the switch and cascode transistors. This reduces C_S roughly by a factor of 2 in a

typical implementation. The amount of improvement is technology dependent.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram for a conventional current switch in prior art current steering DACs.

Figure 2 is a circuit diagram for one embodiment of the present invention.

Figure 3 is a circuit diagram for a preferred embodiment of the present invention.

Figure 4 is an exemplary embodiment of the amplifier A of the embodiments of Figures 2 and 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention takes a different approach. Rather than minimizing the error, the error is sensed, and an opposite error is added, nulling the original error.

A circuit diagram is shown in Figure 2. A capacitor C_C is connected to the common source node of the current switch. The bottom plate of this capacitor is driven by an amplifier A with voltage gain equal to A. The input of amplifier A is driven by the common source node of a replica of the current switch. The replica switch (transistors M_3 and M_4) has the same current density as the "real" current switch (transistors M_1 and M_2), hence it has the same error on the common source node. The amplifier thus senses the error at this node, and injects a compensating charge into the common source node of transistors M_1 and M_2 through the capacitor C_C. The capacitor C_C is driven such that it adds back the charge taken from the signal current source to charge C_S.

The amount of charge to be added to C_S to compensate the error introduced by this capacitance can be calculated as follows. The change in the output voltage seen by the on-switch from one sample to the next can be called Δv. The voltage on the switch common source node will change from V_{CS} to $V_{CS} + \Delta v/(g_m/g_{ds})$, where g_m/g_{ds} is the intrinsic gain of

the switch transistor. Using the charge equations for the circuit, the charge taken from the current source to charge C_S will be replenished if the voltage gain of the amplifier is:

$$A = \frac{C_S + C_C}{C_C}$$

Hence, for example, if $C_C = C_S$, A = 2 is required.

This embodiment may have some limitations. One is that the routing between the current switches and the dummy load needs to go across a large distance, making for a layout challenge. Another problem is that additional accurate current sources are needed for the replica switches (these preferably should be scaled down). Another is that it limits operation of the DAC to a limited range of output impedance for low distortion. If the load impedance of the DAC and the load impedance of the dummy load are different, the charge cancellation will not be complete. This may very well be the case. Typically, one would integrate the dummy load to avoid extra pins for this load, and also to avoid bandwidth reduction caused by ESD structures. The DAC load resistors on the other hand are typically not integrated to maximize the user's flexibility in interfacing with the DAC output. In order to circumvent these limitations, an alternative embodiment is preferred.

The preferred embodiment is illustrated in Figure 3. As shown therein, a current splitter is added in each current source cascode, which already exists as part of each current source. The current of each source is split into two parts, I_1 and I_2. I_2 is scaled down a factor *n*, where *n* is a rational number. Typically, *n* may preferably be larger than 2, and more preferably 4 or more. The remaining current I_1 is the main contribution to the signal current. This is scaled a factor (1-1/n). These currents go to two different switches. The main switch consists of transistors M_1 and M_2. The main switch device width is scaled a factor (1-1/n). The reduced switch consists of transistors M_3 and M_4. The widths of transistors M_3 and M_4 are scaled by a factor of (1/n) compared to the size of the original switch transistors M_1 and M_2. The outputs of the two switches both go to the DAC output. A voltage amplifier with voltage gain = A senses the voltage on the common source node of the reduced or replica switch and injects charge into the common source node of the main switch responsive thereto. In this case, C_C should be chosen a little bit larger than in the case of a dummy switch and dummy loads being used. The reason is that the parasitic capacitance on the common source node of the replica switch (transistors M_3, M_4) is not being compensated. This can be

dealt with by slightly overcompensating the main switch (transistors M_1, M_2).

In operation, when the output voltage starts to change, V_{CS} for both the primary switch and the replica switch begin to change. The change in voltage of the common source node of the replica switch causes amplifier A to amplify the change, in turn causing capacitor C_c to inject an electronic charge into the common source node of the primary switch proportional to the voltage change of the common source node of the replica switch. As pointed out before, the charge can be proportioned to change the voltage across the capacitance C_s for the primary switch, so that no charge to or from the output is required for this purpose. Slightly increasing the charge for a given change in output voltage ΔV can offset the charge required to compensate for the required charging of the common source node of the replica switch. Care should be taken, however, to not have the loop gain through the two on switches, amplifier A and capacitor C_c, including the loading of the parasitic capacitors C_s, exceed unity for stability reasons. In a multistage thermometer coded DAC, the present invention may be implemented in all stages, or alternatively, in the most significant bit stage only.

The buffer amplifier A used for the compensation should have a fast settling step response such that the output

settles before the end of the clock cycle. This means a wide bandwidth. It is also important to have good supply rejection, and that the output be referenced to the same ground as the switch driver. Furthermore, the input of the buffer should have a low capacitance. A buffer implementation satisfying these requirements is shown in Figure 4. Unity gain buffers (followers) are used at the amplifier input to reduce input capacitance and for level shifting. The ratio of $g_{m(MP1)}/g_{m(MP3)}$ is used to set gain. In one embodiment, a bandwidth of approximately 1GHz was found to be sufficient for a 500MHz DAC update rate. To maximize bandwidth, it is important that the current source I_{BIAS} is cascoded to have low output capacitance.

Frequently in MOS circuits, the bodies or bulk of the transistors are each connected to the respective transistor source. However, this is not a limitation in the present invention, as the bodies of the transistors may be connected to another voltage, if desired, provided there is ample protection against forward biasing the inherent body diodes during normal operation. Also, while MOS transistors are preferred, other types of transistors, such as bipolar transistors, may be used if desired.

While certain preferred embodiments of the present invention have been disclosed herein, such disclosure is only

for purposes of understanding the exemplary embodiments and not by way of limitation of the invention. It will be obvious to those skilled in the art that various changes in form and detail may be made in the invention without departing from the spirit and scope of the invention as set out in the full scope of the following claims.